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EXAMINER	
BOLOURCHI, NADER	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/821,649	SONG, HONGJIANG	
	Examiner	Art Unit	
	Nader Bolourchi	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Applicant's amendment to claims is entered.

2. Claims stand rejected under 35 USC § 103.

Response to Arguments

3. The amendment filed 12/18/2006 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "without reference to either the input signal or the output signal" in line 3 of amended claim 1, line 5 of amended claim 10, lines 3-4 of amended claim 16, and lines 7-8 of amended claim 24.

Applicant is required to cancel the new matter in the reply to this Office Action.

4. Applicant's arguments filed 12/18/2006 have been fully considered but they are not persuasive.

Examiner acknowledges that Applicant properly indicated (emphasis added):

The Office Actions states on page 3 that claims 1, 2 and 24-26 are rejected under § 102. However, it appears that the claims are instead rejected under 35 U.S.C. § 103 in view of the combination of Gunzelmann and Pang. Thus, the recitation of "§ 102" in these rejections is considered to be a typographical error.

In response to Applicant's argument in pages 6-8as follow (emphasis added):

Regarding the § 103 rejection of claim 1, as amended, the system of independent claim 1 includes a locked loop circuit to indicate a timing between an input signal and an output signal without reference to the input signal or output signal. The system also includes a processor that controls the locked loop circuit based on the indication of timing.

As conceded by the Examiner, Gunzelmann fails to disclose a processor that controls a locked loop circuit based on the indication of a timing between input and output signals of the locked loop circuit. Office Action, 3. Pang does not supply the missing claim limitations.

Examiner respectfully disagrees. All the limitations disclosed by Pang have been properly addressed in the last office action (emphasis added):

(1) With regard to claim 1, Gunzelmann et al. discloses in (Fig. 7) a locked loop circuit (5, 6); and processor (2) coupled to the locked loop circuit (2, 5, 6) to control the locked loop circuit (Δ_1, 5, Δ_2, 6) and perform at least one other function in the system (3) not related to the control of the locked loop circuit.

However Gunzelmann et al. does not disclose a processor coupled to the locked loop circuit based on the indication of the timing control of the locked loop circuit.

However Pang discloses in (Fig. 2) a processor (20) coupled to the locked loop circuit (22) based on the indication of the timing control of the locked loop circuit (abstract, col. 1, lines 25-31, col. 2, lines 17-19, col. 3, lines 1-12).

Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. to incorporate a processor coupled to the locked loop circuit based on the indication of the timing control of the locked loop circuit in order to provide a microprocessor with a variable clock operation that facilitates use of a maximum operational speed and a lowest operational speed within the operational range (Pang, col. 1, lines 60-63).

Applicant further argues (emphasis added):

> However, Pang fails to teach or suggest either the locked loop circuit of claim 1 or a processor that controls a locked loop circuit based on an indication of a timing (provided by a locked loop circuit) between an input signal and an output signal without reference to the input and output signals. In this regard, although the output signal of the PLL circuit 22 may arguably provide an indication of a timing between the input and output signals when reference to its input signal is made, there is no teaching or suggestion in Pang regarding the PLL circuit 22 providing an indication of the timing without reference to either input or output signal. As such, Pang fails to teach or suggest the missing claim limitations.

Examiner respectfully disagrees. Applicant argument is contradictory, since Applicant claims a locked loop circuit to indicate a timing between an input signal and an output signal, which one can interprets that indication of timing is in reference to input signal and output signal. Furthermore, the specification is silent about such "referencing" and

does not offer any other interpretation. Therefore Examiner has interpreted the phrase "without reference to either the input signal or the output signal" as: the indication of timing is not related to real value of the input signal and the output signal.

Therefore claims 1-15 stand rejected.

Applicant also argues that (emphasis added):

> Regarding the § 103 rejection of claim 16, this claim now recites providing a locked loop circuit that has a processor accessible interface and indicates a timing between an input and an output signal of the locked loop circuit without reference to either the input signal or the output signal. Furthermore, the method of independent claim 16 recites using a processor to control a delay that is introduced by the locked loop circuit between the input and output signals based on the indicated timing.

As stated above, Examiner has interpreted the phrase "without reference to either the input signal or the output signal" as: the indication of timing is not related to real value of the input signal and the output signal.

Therefore, claims 24-29 stand rejected.

Applicant further argues (emphasis added):

> Regarding the § 103 rejections of claims 24-29, as amended, the article of independent claim 24 includes a computer accessible storage medium that stores instructions to, when executed cause a processor to receive an indication of a phase difference from a locked loop circuit. The indication includes an indication of the phase difference without reference to either of the input or output signals of the locked loop circuit. See discussion of independent claim 1 above. Claims 25-29 are patentable for at least the reason that these claims depend from an allowable claim.

As stated above, claim 1 stand rejected. Therefor, claims 24-29 stand rejected due to the same reasoning.

Claim Objections

5. Claims 25-28 are objected to because of the following informalities:

- in first line of claim 25, replace phrase "claim 23" with - -claim 24- -.
- in first line of claims 26-28, replace phrase "the storage" with - -wherein the storage- -

Appropriate correction is required.

Claim Rejections - 35 USC § 112

Claim Rejections - 35 USC § 112, first paragraph

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1, 10, 16, and 24 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The subject matter which is not supported by the original disclosure is as follows: "without reference to either the input signal or the output signal" in line 3 of claim 1, line 5 of claim 10, lines 3-4 of claim 16, and lines 7-8 of claim 24.

Claims 2-9, 11-15, 17-23 and 25-29 are rejected due to their dependency to rejected independent claims 1, 10, 16, and 24 respectively.

Claim Rejections - 35 USC § 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-9 and 16-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 16 in line 3 of claim 1, and lines 3-4 of claim 16 recite "a locked loop circuit to indicate a timing between an input signal and an output signal without reference to either the input signal or the output signal", which term "reference" makes it vague and unclear. It is not clear what term "reference" is referring to. Applicant claims a locked loop circuit to indicate a timing between an input signal and an output signal, which can be properly interpreted as: indication of timing is in reference to input signal and output signal. Furthermore, the specification is silent about such "referencing" and does not offer any other interpretation.

Claims 2-9 and 17-23 are rejected due to their dependency to rejected independent claims 1 and 16 respectively.

8. Claims 10-15, and 24-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject

matter which applicant regards as the invention. Claims 10, and 24 in line 5 of claim 10, and lines 7-8 of claim 24 recite "a phase detector to indicate a phase difference between the input clock signal and the output clock signal without reference to either the input signal or the output signal" (Examiner notes the difference in wording of claim 24), which term "reference" makes it vague and unclear. It is not clear what term "reference" is referring to. Applicant claims a locked loop circuit to indicate a phase difference between the input clock signal and the output clock signal, which can be properly interpreted as: indication of phase difference is in reference to the input clock signal and the output clock signal. Furthermore, the specification is silent about such "referencing" and does not offer any other interpretation.

Claims 11-15 and 25-29 are rejected due to their dependency to rejected independent claims 10 and 24 respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 2, and 24-26 are rejected under 35 U.S.C. 103(a) as being anticipated by Gunzelmann et al. (US Patent 6,532,255) in view of Pang (US Patent 6,477,658).

Regarding claim 1, Gunzelmann et al. discloses in (Fig. 7) a locked loop circuit (5, 6); and processor (2) coupled to the locked loop circuit (2, 5, 6) to control the locked loop circuit (A1, 5, A2, 6) and perform at least one other function in the system (3) not related to the control of the locked loop circuit. Gunzelmann et al. does not disclose a processor coupled to the locked loop circuit based on the indication of the timing control of the locked loop circuit.

Pang discloses in (Fig. 2) a processor (20) coupled to the locked loop circuit (22) based on the indication of the timing control of the locked loop circuit (abstract, col. 1, lines 25-31, col. 2, lines 17-19, col. 3, lines 1-12) without reference to either the input signal or the output signal (Examiner notes that the indication of timing is not related to real value of the input signal and the output signal). Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. to incorporate a processor coupled to the locked loop circuit based on the indication of the timing control of the locked loop circuit in order to provide a microprocessor with a variable clock operation that facilitates use of a maximum operational speed and a lowest operational speed within the operational range as suggested by Pang (col. 1, lines 60-63).

Regarding claim 2, Gunzelmann et al. and Pang disclose as stated in rejection of claim 1 above. Gunzelmann et al. further discloses in (Fig. 7) that the locked loop circuit comprises a delay locked loop circuit (5, 6).

Regarding claim 24, Gunzelmann et al. and Pang disclose as stated in rejection of claim 1 above. Pang further discloses in (Fig. 2) an article comprising a computer accessible storage medium storing instructions (26), when executed cause a processor

(20) to: receive indication of phase difference from a locked loop circuit (col. 3, liens 56-67 - col. 4, lines 1-15) and control the locked loop circuit (22) without reference to either the input signal or the output signal (Examiner notes that the indication of a phase difference is not related to real value of the input signal and the output signal). Therefore, It would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teaching of Gunzelmann et al. and Pang for the purpose of providing a microprocessor with a variable clock operation that facilitates use of a maximum operational speed and a lowest operational speed within the operational range as suggested by Pang (col. 1, lines 60-63).

Regarding claim 25, Gunzelmann et al. and Pang disclose as stated in rejection of claim 24 above. Gunzelmann et al. further discloses that the locked loop circuit comprises a delay locked loop circuit (Fig. 7: (5, 6)).

Regarding claim 26, Gunzelmann et al. and Pang disclose as stated in rejection of claim 25 above. Gunzelmann et al. further discloses (Fig. 7) the storage medium storing instructions to cause the processor (2) to use the interface to receive the indication of the phase difference (5, 6, 2, T1, T2).

10. Claims 3, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunzelmann et al. (US Patent 6,532,255) in view of Pang (US Patent 6,477,658i, as applied to claims 1 and 2, and further in view of Leonida (US Patent 5,353,025).

Regarding claim 3, Gunzelmann et al. and Pang disclose as stated in rejection of claim 1 above. However, they do not disclose that the locked loop circuit comprises an interface accessible by the processor.

Leonida discloses that the locked loop circuit comprises an interface accessible by the processor (Fig. 2 (116, 162, 118), Fig. 3 (118, 162, 182, 233)) (col. 5, lines 66-68 - col. 6, lines 3-8, col. 7, lines 65-68 - col. 8, lines 1-2). Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. in combination with Pang in view of Leonida to incorporate the locked loop circuit which comprises an interface accessible by the processor in order to provide a variable delay with respect to the start of the circuit board operation (Leonida, col. 6, lines 53-59).

Regarding claim 16, Gunzelmann et al. Pang, and Leonida disclose as stated in rejection of claims 1 and 3 above. Gunzelmann et al. in combination with Pang and Leonida disclose all the limitations of claim 16, as stated in rejection of claims 1 and 3 above.

Regarding claim 17, Gunzelmann et al. Pang, and Leonida disclose as stated in rejection of claims 16 and 2 above. Gunzelmann et al. in combination with Pang and Leonida disclose all the limitations of claim 17, as stated in rejection of claims 16 and 2 above.

11. Claims 4-6, 18-21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunzelmann et al. (US Patent 6,532,255) in view of Pang (US Patent 6,477,658) in view of Leonida (US Patent 5,353,025), as applied to claims 1 and 3, and further in view of Silvestri (US Patent Application 2002/0130691 A1).

Regarding claim 4, Gunzelmann et al., Pang, and Leonida disclose as stated in rejection of claim 3 above. However, they not disclose that the interface indicates a

phase difference between an input clock signal and an output clock signal generated by the locked loop circuit.

Silvestri discloses in (Fig. 2 (54)) that the interface indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit (Fig. 3, pg. 3, col. 2, lines 22-49). Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. in combination Pang in combination with Leonida in view of Silvestri to incorporate wherein the interface indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit in order to provide a memory device having a circuit which dynamically locks a DLL in a minimum number of cycles, which would provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

Regarding claim 5, Gunzelmann et al., Pang, and Leonida disclose as stated in rejection of claim 3 above. However, they are silent about computer system.

Silvestri discloses in (Fig. 1) that the system comprises a computer system (26) having a system memory (Fig. 2 (38)) and the interface (Fig. 2 (12)) is addressable (Fig. 2 (34)) in a range of addresses used to access the system memory (Pg. 2, col. 2, lines 5-24, pg. 3, col. 1, lines 6-41). Therefore it would have been obvious to one of ordinary skill in the art combine the teaching of Gunzelmann et al., Pang, and Leonida with Silvestri to incorporate the interface that indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit in order to provide a memory device having a circuit which dynamically locks a DLL in a minimum number of cycles, which would provide a locking method and apparatus which coincides

with the ever-increasing speed of microprocessing and memory access, as suggested by Silvestri (Pg. 1, col. 2, lines 46-50).

Regarding claim 6, Gunzelmann et al., Pang, and Leonida disclose as stated in rejection of claim 3 above. However, they are silent about the interface indicates storage accessible by the processor.

Silvestri further discloses in (Fig. 2 (54, 12), Fig. 3 (62)) wherein the interface indicates storage accessible by the processor to store an indication of a delay used by the locked loop circuit (Pg. 3, col. 2, lines 51-67). Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. in combination Pang in combination with Leonida in view of Silvestri to incorporate wherein the interface indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit in order to provide a memory device having a circuit which dynamically locks a DLL in a minimum number of cycles, which would provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

Regarding claim 18, Gunzelmann et al. and Pang disclose as stated in rejection of claims 16. However, they are silent about read and write operation to the interface.

Silvestri further discloses in (Fig. 2 (30)) performing at least one of read and writes operations to the interface to control the locked loop circuit (Pg. 3, col. 1, lines 51-61, col. 2, lines 10-20). Therefore it would have been obvious to one of ordinary skill in the art to combine teaching of Dvorak et al. and Pang with Silvestri in order to provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

Regarding claim 19, Gunzelmann et al. and Pang, Leonida, and Silvestri disclose as stated in rejection of claims 16 and 4 above. Gunzelmann et al. and Pang, Leonida, in combination with Silvestri disclose all the limitations of claim 19, as stated in rejection of claims 16 and 4 above.

Regarding claim 20, Gunzelmann et al. and Pang, Leonida, and Silvestri disclose as stated in rejection of claims 16 and 5 above. Gunzelmann et al. and Pang, Leonida, in combination with Silvestri disclose all the limitations of claim 20, as stated in rejection of claims 16 and 5 above.

Regarding claim 21, Gunzelmann et al. and Pang, Leonida, and Silvestri disclose as stated in rejection of claims 16 and 6 above. Gunzelmann et al. and Pang, Leonida, in combination with Silvestri disclose all the limitations of claim 21, as stated in rejection of claims 16 and 6 above.

Regarding claim 23, Gunzelmann et al. and Pang, Leonida, and Silvestri disclose as stated in rejection of claims 16 and 8 above. Gunzelmann et al. and Pang, Leonida, in combination with Silvestri disclose all the limitations of claim 23, as stated in rejection of claims 16 and 8 above.

12. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunzelmann et al. (US Patent 6,532,255) in view of Pang (US Patent 6,477,658), as applied to claims 1, and further in view of Silvestri (US Patent Application 2002/0130691 A1).

Regarding claim 8, Gunzelmann et al. and Pang disclose as stated in rejection of claim 1 above. However, they are silent about microprocessor.

Silvestri discloses in (Fig. 1 (12), Fig. 2 (12)) wherein the processor comprises a microprocessor (Pg. 2, col. 1, lines 34-41). Therefore it would have been obvious to one of ordinary skill in the art to combine teaching of Gunzelmann et al. and Pang as stated in claim 1, in combination with Silvestri to incorporate wherein the interface indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit in order to provide a memory device having a circuit which dynamically locks a DLL in a minimum number of cycles, which would provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

Regarding claim 9, Gunzelmann et al. and Pang disclose as stated in rejection of claim 1 above. However, they are silent about system memory

Silvestri discloses a system memory storing a program; wherein the processor executes the program to perform said other function (Pg. 2, col. 2, lines 5-24). Therefore it would have been obvious to one of ordinary skill in the art to combine teaching of Gunzelmann et al. and Pang as stated in claim 1, in combination with Silvestri to incorporate wherein the interface indicates a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit in order to provide a memory device having a circuit which dynamically locks a DLL in a minimum number of cycles, which would provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

13. Claims 7, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunzelmann et al. (US Patent 6,532,255) in view of Pang (US Patent 6,477,658) in view of Leonida (US Patent 5,353,025), in view of Silvestri (US Patent Application 200210130691 A1), as applied to claims 3, 16, 24 in further view of Dvorak et al. (US Patent 6,535,989).

Regarding claim 7, Gunzelmann et al., Pang, and Leonida disclose as stated in rejection of claim 3 above. However, they do not disclose wherein the interface includes storage accessible by the processor to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit.

Dvorak et al. discloses in (Fig. 3 (500)) wherein the interface includes storage accessible by the processor (Fig. 5 (500, 515)) to store an indication of a selection (505) of one or more of a plurality of output clock signals furnished by the locked loop circuit (abstract, col. 1, lines 15-26, 57-60, col. 4, lines 10-35, col. 6, lines 43-48). Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. in combination Pang in combination with Leonida in combination with Silvestri in view of Dvorak et al. to incorporate wherein the interface includes storage accessible by the processor to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit in order to provide a PLL that can handle variable core-bus clock frequency ratios and not have to re-lock every time the ratio changes (Dvorak, col. 2, lines 19-26).

Regarding claim 22, Gunzelmann et al. Pang, Leonida, Silvestri, and Dvorak disclose as stated in rejection of claims 16 and 7 above. Gunzelmann et al. and Pang,

Leonida, Silvestri in combination with Dvorak disclose all the limitations of claim 22, as stated in rejection of claims 16 and 7 above.

Regarding claim 28, Gunzelmann et al. and Pang disclose as stated in rejection of claim 24 above. However they are silent about what storage medium storing.

Dvorak et al. further discloses in (Fig. 3 (500)) wherein the interface includes storage accessible by the processor (Fig. 5 (500, 515)) to store an indication of a selection (505) of one or more of a plurality of output clock signals furnished by the locked loop circuit (abstract, col. 1, lines 15-26, 57-60, col. 4, lines 17-35, col. 6, lines 43-48). Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. in combination Pang in combination with Leonida in combination with Silvestri in view of Dvorak et al. to incorporate wherein the interface includes storage accessible by the processor to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit in order to provide a PLL that can handle variable core-bus clock frequency ratios and not have to re-lock every time the ratio changes (Dvorak, col. 2, lines 19-26).

14. Claim 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dvorak et al. (US Patent 6,535,989) in view of Pang (US Patent 6,477,658).

Regarding claim 10, Dvorak et al. discloses a locked loop circuit comprising (Fig. 3, Fig. 4): a delay line (305-(1-8)) to receive an input clock signal and furnish an output clock signal; a phase detector (310) to indicate a phase difference between the input clock signal and the output clock signal (col. 1, lines 24-61, col. 3, lines 57-62, col. 4, lines 5-12). However, Dvorak does not disclose an interface accessible by a processor

to control the locked loop circuit to adjust a timing between the input clock signal and the output clock signal based on the indicated phase difference.

Pang discloses in (Fig. 2) an interface (25) accessible by a processor (20) to control the locked loop circuit (22) to adjust a timing between the input clock signal and the output clock signal based on the indicated phase difference (abstract, col. 1, lines 25-31, col. 2, lines 17-19, col. 3, lines 1-12, 56-67 - col. 4, lines 1-14) without reference to either the input signal or the output signal (Examiner notes that the indication of a phase difference is not related to real value of the input signal and the output signal). Therefore it would have been obvious to one of ordinary skill in the art to modify Dvorak et al. in view of Pang to incorporate an interface accessible by a processor to control the locked loop circuit to adjust a timing between the input clock signal and the output clock signal in order to provide a microprocessor with a variable clock operation that facilitates use of a maximum operational speed and a lowest operational speed within the operational range (Pang, col. 1, lines 60-63).

Regarding claim 15, Dvorak et al. in combination with Pang disclose as stated in rejection of claim 10 above.

Dvorak et al. further discloses in (Fig. 3 (500)) that the interface includes storage accessible by the processor (Fig. 5 (500, 515)) to store an indication of a selection (505) of one or more of a plurality of output clock signals furnished by the locked loop circuit (abstract, col. 1, lines 15-26, 57-60, col. 4, lines 10-35, col. 6, lines 43-48).

15. Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dvorak et al. (US Patent 6,535,989) in view of Pang (US Patent 6,477,658) as applied to claim 10, in further view of Gunzelmann et al. (US Patent 6,532,255).

Regarding claim 11, Dvorak et al. in combination with Pang disclose as stated in rejection of claim 10 above. However they do not disclose that the locked loop circuit comprises a delay locked loop circuit.

Gunzelmann et al. discloses in (Fig. 7 (5, 6)) wherein the locked loop circuit comprises a delay locked loop circuit. Therefore it would have been obvious to one of ordinary skill in the art to modify the inventions of Dvorak et al. in combination with Pang in view of Gunzelmann et al. to incorporate wherein the locked loop circuit comprises a delay locked loop circuit in order to slave the phase angle of the locally produced spread sequence as accurately as possible to the directly received signal once the signal has been acquired (Gunzelmann et al., col. 2, lines 30-34).

16. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dvorak et al. (US Patent 6,535,989) in view of Pang (US Patent 6,477,658), and further in view of Silvestri (US Patent Application 2002/0130691 A1).

Regarding claim 12, Dvorak et al. and Pang disclose as stated in rejection of claim 10 above. However they are silent about the interface indicating phase difference.

Silvestri discloses in wherein the interface indicates a phase difference between an incoming clock signal to the locked loop circuit and another signal generated by the locked loop circuit (Pg. 3, col. 2, lines 22-49). Therefore it would have been obvious to one of ordinary skill in the art to combine teaching of Dvorak et al. and Pang with

Silvestri in order to provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

Regarding claim 13, Dvorak et al. and Pang disclose as stated in rejection of claim 10 above. However they are silent about the interface accessing the memory.

Silvestri further discloses in (Fig. 1) wherein the system comprises a computer system (26) having a system memory (Fig. 2 (38)) and the interface (Fig. 2 (12)) is addressable (Fig. 2 (34)) in a range of addresses used to access the system memory (Pg. 2, col. 2, lines 5-24, pg. 3, col. 1, lines 6-41). Therefore it would have been obvious to one of ordinary skill in the art to combine teaching of Dvorak et al. and Pang with Silvestri in order to provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

Regarding claim 14, Dvorak et al. and Pang disclose as stated in rejection of claim 10 above. However they are silent about interface having storage accessible by the processor.

Silvestri further discloses wherein the interface includes storage accessible by the processor to store an indication of a delay applied by the locked loop circuit to the input clock signal (Fig. 2 (54, 12), Fig. 3 (56, 58)). Therefore it would have been obvious to one of ordinary skill in the art to combine teaching of Dvorak et al. and Pang with Silvestri in order to provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

17. Claims 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gunzelmann et al. (US Patent 6,532,255) in view of Pang (US Patent 6,477,658i, as applied to claims 1 and 2, and further in view of Dvorak et al. (US Patent 6,535,989).

Regarding claim 29, Gunzelmann et al. and Pang disclose as stated in rejection of claim 1 above. See rejection of claim 10. However, they are silent about storage in the interface.

Dvorak et al. discloses the delay locked loop circuit (Fig. 3, Fig. 4) comprises a delay chain to establish a delay between the input signal and the output signal line (305-(1-8)), and the processor (Fig. 2: 20) controls the delay chain (Fig. 2:22) based on the indicated timing between the input signal and the output signal (abstract, col. 1, lines 25-31, col. 2, lines 17-19, col. 3, lines 1-12, 56-67 - col. 4, lines 1-14).

Therefore it would have been obvious to one of ordinary skill in the art to combine teaching of Gunzelmann et al. and Pang with Dvorak et al use a processor to control the locked loop circuit to adjust a timing between the input clock signal and the output clock signal in order to provide a microprocessor with a variable clock operation that facilitates use of a maximum operational speed and a lowest operational speed within the operational range, as suggested by Pang (col. 1, lines 60-63).

18. Claim 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunzelmann et al. (US patent 6,532,255) in view of Pang (US Patent 6,477,658), as applied to claim 24, and further in view of Silvestri (US Patent Application 2002/0130691).

With regard to claim 27, Gunzelmann et al. and Pang disclose as stated in rejection of claim 24 above. However they do not disclose the storage medium storing instructions to cause the processor to store an indication of a delay used by the locked loop circuit in an interface of the locked loop circuit.

Silvestri discloses in (Fig. 1, Fig. 2) the storage medium storing instructions to cause the processor to store an indication of a delay used by the locked loop circuit in an interface of the locked loop circuit ((Fig. 2 (12, 34, 54), Pg. 2, col. 2, lines 5-24, pg. 3, col. 1, lines 6-41). Therefore it would have been obvious to one of ordinary skill in the art to modify Gunzelmann et al. in view of Silvestri to incorporate the storage medium storing instructions to cause the processor to store an indication of a delay used by the locked loop circuit in an interface of the locked loop circuit in order to provide a memory device having a circuit which dynamically locks a DLL in a minimum number of cycles, which would provide a locking method and apparatus which coincides with the ever-increasing speed of microprocessing and memory access (Silvestri, Pg. 1, col. 2, lines 46-50).

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

21. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nader Bolourchi whose telephone number is (571) 272-8064. The examiner can normally be reached on M-F 8:30 to 4:30.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David. C. Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

Nader Bolourchi
3/8/2007
Art Unit 2611

JEAN B. CORRIELUS
PRIMARY EXAMINER
3-19-07